

**IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
AUSTIN DIVISION**

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

**Lead Case:** 1:19-cv-977-ADA

*(Consolidated with Nos. 6:19-cv-254-  
ADA, 6:19-cv-255-ADA, 6:19-cv-256-  
ADA)*

**VLSI TECHNOLOGY LLC'S CLAIM CONSTRUCTION PROPOSAL**  
**U.S. PATENT NO. 7,292,485**

VLSI proposes the following plain and ordinary meaning construction: **"a structure that is used to provide capacitance."**

Exemplary intrinsic evidence underscoring that capacitance can be provided by a variety of structures including capacitors and transistors—not just dummy memory cells—is attached hereto for the Court's convenience as Exhibits A-D and includes:

- *Compare* '485 Patent (Ex. A), cl. 1 ("a first capacitance structure includes a plurality of dummy cells"), *with* '485 Patent, cl. 17 ("a capacitance structure;") (differentiating capacitance structures with and without dummy cells required)
- '485 Patent Prosecution History: August 6, 2007 Supplemental Notice of Allowability (Ex. B) ("An examiner's amendment to the record appears below. . . . In claim 1, line 5, after the word 'structure', the words --includes a plurality of dummy cells-- have been inserted. . . . In claim 12, line 6, after the word 'structure', the words --includes a plurality of dummy cells-- have been inserted.") (inserting, in an examiner's amendment, "includes a plurality of dummy cells" after "capacitance structure" in claims 1 and 12, but not claims 9 and 17, indicating that a "capacitance structure" alone is not limited to dummy cells)
- U.S. Patent No. 4,094,008 (cited art) (Ex. C), *e.g.*, at Abstract and cl. 1 (titled "Alterable **Capacitor** Memory Array," disclosing "A novel memory array . . . , the array utilizing a matrix of variable threshold insulated gate field effect **transistor cells**. . . . In operation, **each cell functions as an alterable capacitor**. . . . Variations in stored charge at the nitride-oxide interface causes changes in the threshold voltage and effective **capacitance of the cell**," and claiming a "memory system comprising: a rectangular array of non-volatile, alterable threshold **capacitors** . . . , and a plurality of non-volatile, alterable-threshold **capacitor devices** . . . ") (discussing use of capacitors and transistor cells to provide capacitance)
- U.S. Patent No. 5,894,433 (cited art) (Ex. D), *e.g.*, at 18:33-36 ("Since the signal  $\Phi P1$  is a high voltage (VCH) pulse, however, the power for charging/discharging the gate **capacitance of the numerous switch MOS transistors** connected to that line is relatively increased.") (discussing use of transistors to provide capacitance)
- '485 Patent (Ex. A) at 2:20-21 ("Also, the **amount of charge shared** is programmable by selecting how many **dummy cells** are connected . . . ") (indicating that the "dummy **cells**" are the structure associated with capacitance sharing in this embodiment, not dummy columns or rows as Intel suggests); *see also, e.g.*, '485 Patent at 4:5-7 ("The amount of capacitance shared is determined in part by how many memory cells are coupled to conductor 37."); '485 Patent at 4:44-46 ("The **capacitance** of dummy column 17 can be adjusted by selecting the number of **memory cells** coupled to conductor 37")

Dated: December 19, 2019

Respectfully submitted,

By: /s/ Charlotte J. Wen

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**CERTIFICATE OF SERVICE**

A true and correct copy of the foregoing instrument was served or delivered electronically via U.S. District Court [LIVE] — Document Filing System, to all counsel of record, on this 19th day of December, 2019.

/s/ Charlotte J. Wen

Charlotte J. Wen (*pro hac vice*)